EEPROM CELL USING CONVENTIONAL PROCESS STEPS

ABSTRACT OF THE DISCLOSURE

An EEPROM cell (10) formed on a substrate (18) using conventional process steps is provided. The cell (10) includes first (12) and second (14) conductive regions in the substrate (18) below the substrate's outer surface (28), and the first (12) and second (14) conductive regions are laterally displaced from one another by a predetermined distance (32). The cell (10) also includes an insulating layer (20) outwardly from the outer surface (28) of the substrate (18) positioned so that its edges are substantially in alignment between the first (12) and second (14) conductive regions. The cell (10) further includes a floating gate layer (22) outwardly from the insulating layer (20) and in substantially the same shape as the insulating layer (20). The cell (10) also includes a diffusion region (24 or 26) that extends laterally from at least one of the first (12) and second (14) conductive regions so as to overlap with the insulating layer (20). The diffusion region (24 or 26) provides a source of charge for placement on the floating gate layer (22) when programming the EEPROM cell (10).